REMARKS

This Amendment responds to the Office Action dated May 30, 2006 in which the Examiner rejected claims 1-2, 5-6 and 8-9 under 35 U.S.C. §103.

As indicated above, claims 1, 5 and 6 have been amended in order to make explicit what is implicit in the claims. The amendment is unrelated to a statutory requirement for patentability.

Claim 1 claims a microcomputer comprising a memory, a central processing unit, and a functional block comprising a peripheral block, built-in the microcomputer. The memory has a reprogrammable nonvolatile memory storing user data, and in which a lock code is written in a specified area. The microcomputer comprises first and second decoding circuits and a logic circuit. The first decoding circuit is connected with the nonvolatile memory, which reads out the lock code, and decodes the lock code. The logic circuit performs a predetermined operation on an externally input mode bit, by the output from the first decoding circuit. The second decoding circuit decodes the processed mode bit by receiving the output from the logic circuit, and sends the obtained results to the functional block. The lock code comprises a plurality of bits and has a priority. An operation mode of the microcomputer is changed according to the lock code.

Through the structure of the claimed invention having a lock code comprising a plurality of bits and a priority and having an operation mode of the microcomputer changed according to the lock code, as claimed in claim 1, the claimed invention provides a microcomputer which cannot be arbitrarily accessed. The prior art does not show, teach or suggest the invention as claimed in claim 1.

Claim 5 claims a microcomputer comprising a memory, a central processing unit, a functional block comprising a peripheral block, built-in the microcomputer, and an external terminal. The memory comprises a reprogrammable nonvolatile memory storing user data, and in which a function-selecting code for selecting the function of the external terminal is written in a specified area. The microcomputer comprises a first decoding circuit connected with the nonvolatile memory, which reads out the function-selecting code and decodes this code; and a selector circuit that selects a function of the external terminal by receiving the output from the first decoding circuit. The nonvolatile memory stores a lock code, and the lock code comprises a plurality of bits and has a priority. An operation mode of the microcomputer is changed according to the lock code.

Through the structure of the claimed invention having a lock code comprising a plurality of bits and a priority and having an operation mode of the microcomputer changed according to the lock code, as claimed in claim 5, the claimed invention provides a microcomputer which can limit the function of an external terminal. The prior art does not show, teach or suggest the invention as claimed in claim 5.

Claim 6 claims a microcomputer comprising a memory, a central processing unit, and a functional block comprising a peripheral block, built-in the microcomputer. The memory comprises a reprogrammable nonvolatile memory storing user data, and in which a limiting code for limiting a command is written in a specified area. The microcomputer comprises a first decoding circuit connected with the nonvolatile memory, which reads out the limiting code, and decodes this code; and a second decoding circuit that limits a command to be used, by the output from the first decoding circuit. The nonvolatile memory stores a lock code, and the lock code

comprises a plurality of bits and has a priority. An operation mode of the microcomputer is changed according to the lock code.

Through the structure of the claimed invention having a lock code comprising a plurality of bits and a priority and having an operation mode changed according to the lock code, as claimed in claim 6, the claimed invention provides a microcomputer which can prevent false writings and intentional reprogramming by users. The prior art does not show, teach or suggest the invention as claimed in claim 6.

Claims 1-2, 5-6 and 8 were rejected under 35 U.S.C. §103 as being unpatentable over *Sibigtroth et al* (U.S. Patent No. 5,251,304) and Official Notice.

Sibigtroth et al appears to disclose security of information stored in memory used by data processors. (Column 1, lines 10-11). Shown in FIG. 1 is a block diagram of a data processing system 10, comprised generally of a single integrated circuit package portion 11 and a peripheral portion 12 having an external peripheral device. The integrated circuit package portion 11 has a memory 13, a data processor 14, a decoder 16, an instruction inhibit circuit 18, and a programmable security device 20. (Column 2, lines 18-25). In the illustrated form, an active signal is a logic high signal. The Enable signal provided by programmable security device 20 is activated when the data processing system 10 of FIG. 1 is to operate in the secure mode in response to the Control signal. Programmable security device 20 may be implemented as any type of nonvolatile storage device meaning that the state of the Enable signal remains valid even if power is removed from data processing system 10. Therefore, in one form programmable security device 20 may be implemented with a nonvolatile memory. (Column 3, line 64 through column 4, line 6).

Thus, *Sibigtroth et al.* merely discloses an enable signal. Nothing in *Sibigtroth et al.* shows, teaches or suggests a lock code comprising a plurality of bits and having a priority as claimed in claim 1, 5 and 6. Rather, *Sibigtroth et al.* merely discloses an enable signal output by a programmable security device 20.

Additionally, *Sibigtroth et al.* merely discloses three modes of operating the system based upon control signals. Nothing in *Sibigtroth et al.* shows, teaches or suggests an operation mode of a microcomputer is changed according to the lock code as claimed in claim 1, 5 and 6. Rather, *Sibigtroth et al.* has different modes of operation based upon different control signals and not based only on a lock code.

Official Notice by the Examiner merely states that reconfigurable nonvolatile memories are well known. Thus nothing in the *Official Notice* shows, teaches or suggests a lock code comprises a plurality of bits and has a priority and an operation mode of the microcomputer is changed according to the lock code as claimed in claims 1, 5 and 6.

Since nothing in *Sibigtroth et al.* and *Official Notice* shows, teaches or suggests a) a lock code comprising a plurality of bits and has a priority and b) an operation mode of the microcomputer is changed according to the lock code as claimed in claims 1, 5 and 6, Applicant respectfully requests the Examiner withdraws the rejection to claims 1, 5 and 6 under 35 U.S.C. §103.

Claims 2 and 8 depend from claim 1 and recite additional features. Applicant respectfully submits that claims 2 and 8 would not have been obvious within the meaning of 35 U.S.C. §103 over *Sibigtroth et al.* and *Official Notice* at least for the reasons as set forth above. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claims 2 and 8 under 35 U.S.C. §103.

Claim 9 was rejected under 35 U.S.C. §103 as being unpatentable over *Sibigtroth et al.*

Applicant respectfully traverses the Examiner's rejection of claim 9 under 35 U.S.C. §103. The claim has been reviewed in light of the Office Action, and for reasons which will be set forth below, Applicant respectfully requests the Examiner withdraws the rejection to the claim and allows the claim to issue.

As discussed above, since nothing in *Sibigtroth et al.* shows, teaches or suggests the primary features as claimed in claim 1, Applicant respectfully submits that nothing in the primary reference in combination with *Official Notice* will overcome the deficiencies thereof. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claim 9 under 35 U.S.C. §103.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is requested to contact, by telephone, the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicant respectfully petitions for an appropriate extension of time. The fees for such extension of time may be charged to Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

BUCHANAN INGERSOLL & ROONEY PC

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